St. PETER'S UNIVERSITY

St. Peter's Institute of Higher Education and Research
(Declared under section 3 of UGC Act 1956)
Avadi, Chennai – 600 054.

M.E. (APPLIED ELECTRONICS) PROGRAMME

(I TO IV SEMESTERS)

REGULATIONS AND SYLLABI

(REGULATIONS – 2012)

St. Peter's University

Chennai – 600 054.

M.E. (APPLIED ELECTRONICS) PROGRAMME

Regulations and Syllabi

(Effective from 2012)

1. **Eligibility:** Candidates who passed B.E/B.Tech.(ECE/EIE/EEE/Electronics/ETE)/ AMIE/AMIETE/DMIT of the University or any other equivalent examination thereto are eligible for admission to Two Year M.E. (Applied Electronics) Programme.
2. **Duration:** Two Years Comprising 4 Semesters. Each semester has a minimum 90 working days with a minimum of 5 hours a day.
3. **Medium:** English is the medium of instruction and examination.
4. **Weightage for Internal and End Assessment:** The weightage for Internal Assessment (IA) and End Assessment (EA) be 25:75 unless the ratio is specifically mentioned in the scheme of Examinations.
5. **Credit System:** Credit system be followed with 18 credits for each semester and each credit is equivalent to 25-30 hours of effective study provided in the Time Table.
6. **Scheme of Examinations(for I and II Semesters)**

I Semester

Code No.	Course Title	Credit	Marks		
Theory			**IA**	**EA**	**Total**
112AEPT01	Applied Mathematics	2	25	75	100
112AEPT02	Computer Architecture and Parallel Processing	3	25	75	100
112AEPT03	Advanced Digital Signal Processing	3	25	75	100
112AEPT04	VLSI Design	2	25	75	100
112AEPT05	Computer Communication and Networking	3	25	75	100
108AEPT06	Advanced Micro Processors and Microcontrollers	3	25	75	100
Practical					
112AEPP07	Applied Electronics Lab - I	2	25	75	100
	Total	**18**	**175**	**525**	**700**

II Semester

Code No.	Course Title	Credit	Marks		
Theory			**IA**	**EA**	**Total**
212AEPT01	Analysis and Design of Analog Integrated Circuits	3	25	75	100
212AEPT02	Advanced Digital System Design	3	25	75	100
212AEPT03	Digital Control Engineering	2	25	75	100
212AEPT04	Embedded Systems	2	25	75	100
212AEPT05	High Performance Communication Networks	3	25	75	100
212AEPT06	Digital Image Processing	3	25	75	100
Practical					
212AEPP07	Electronic Design Lab II	2	25	75	100
	Total	**18**	**175**	**525**	**700**

III Semester

Code No.	Course Title	Credit	Marks		
Theory			**CA**	**EA**	**Total**
312AEPT01	Electromagnetic Interference and Compatibility in System Design	2	25	75	100
312AEPT02	Wireless Networks	2	25	75	100
312AEPT03	Neutral Networks and its Applications	2	25	75	100
312AEPP01	Project Work – Phase – I***	12	50	150	200
	Total	**18**	**75**	**225**	**500**

IV Semester

Code No.	Course Title	Credit	Marks		
Project			**CA**	**EA**	**Total**
412AEPP01	Project Work (Phase – II)	18	100	300	400
	Total	**18**	**100**	**300**	**400**

7. Passing Requirements: The minimum pass mark (raw score) be 50% in End Assessment (EA) and 50% in Continuous Assessment (CA) and End Assessment (EA) put together. No minimum mark (raw score) in Continuous Assessment (CA) be prescribed unless it its specifically mentioned in the scheme of Examination.

8. Grading System: Grading System on a 10 Point Scale be followed with 1 mark = 0.1 Grade point to successful candidates as given below.

CONVERSION TABLE

(1 mark = 0.1 Grade Point on a 10 Point Scale)

Range of Marks	Grade Point	Letter Grade	Classification
90 to 100	9.0 to 10.0	O	First Class
80 to 89	8.0 to 8.9	A	First Class
70 to 79	7.0 to 7.9	B	First Class
60 to 69	6.0 to 6.9	C	First Class
50 to 59	5.0 to 5.9	D	Second Class
0 to 49	0 to 4.9	**F**	**Reappearance**

Procedure for Calculation

Cumulative Grade Point Average (CGPA) = $\frac{\text{Sum of Weighted Grade Points}}{\text{Total Credits}}$

= $\frac{\sum (CA+EA)\, C}{\sum C}$

Where Weighted Grade Points in each Course = Grade Points (CA+EA) multiplied by Credits

= (CA+EA)C

Weighted Cumulative Percentage of Marks(WCPM) = CGPAx10

C- Credit, CA-Continuous Assessment, EA- End Assessment

9. Pattern of the Question Paper: The question paper for End Assessment will be set for three hours and for the maximum of 100 marks with following divisions and details.

Part A: 10 questions (with equal distribution to all units in the syllabus). Each question carries 2 marks.

Part B: 5 question with either or type (with equal distribution to all Units in the syllabus). Each question carries 16 marks.

The total marks scored by the candidates will be reduced to the maximum prescribed in the Regulations.

DATE: **Registrar**

10. Syllabus

I Semester

112AEPT01 – APPLIED MATHEMATICS

1. CALCULUS OF VARIATION

Introduction – Euler's equation – several dependent variables Lagrange's equation of Dynamics – Integrals involving derivatives higher that the first – Problem with constrains – Direct methods and eigen value problems.

2. MATRIX THEORY

Eigen values using QR transformations – generalized eigenvectors – canonical forms – singular value decomposition and applications – pseudo inverse – least square.

3. LINEAR PROGRAMMING PROBLEM

Graphical method – simplex method – Big M Technique – Integer programming.

4. LINEAR ALGEBRAIC EQUATION AND EIGEN VALUE PROBLEM

System of Equation – Solution by Gauss Elimination, Gauss-Jordan and LU decomposition method – Jacobi, Gauss – Seidal iteration Method – Eigen Value of matrix by Jacobi and power method.

5. QUEUING THEORY

Single and multiple server Markovian Quening Models – Steady state system size probabilities – Little's formula – customer im patience – priority queues – M/G/I Queuing system – P-K formula.

REFERENCES:

1. Gupta, A.S., Calculus of Variations with Applications, Prentice – Hall of India New Delhi, 1997.
2. Bronson.R, "Matrix Operation", Schaums Outline Series, Mc Graw Hill, Newyork, 1989.
3. Taha H.A, "Operation Research-An Introduction", Prentice Hall of India, 2001.
4. Jain M.K. Iyengar. S.R.K and Jain R.K, "Numerical Methods for Scientific and Engineering computation, "New age international (P) Ltd., Publishers, 2003.

112AEPT02 – COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

UNIT I – MEMORY ORGANIZATION

Memory hierarchy technology – Addressing schemes for main memory – Virtual memory technology – memory management – Back plane bus systems – Cache memory organization – Shared memory organization.

UNIT II – PIPELINING AND SUPERSCALAR

Principles of Linear pipelining – Classification of Pipelined processors – Interleaved memory organization – Instruction and Arithmetic pipelines – Designing pipelined processors – Superscalar processors.

UNIT III – THEORY OF PARALLELISM

Parallel computer models – the state of computing – Multiprocessors and Multicomputers – Multivector and SIMD Computers – PRAM and VLSI Models.

UNIT IV – PROGRAM AND NETWORK PROPERTIES, SCALABLE PERFORMANCE

Conditions of Parallelism – Program Partitioning and scheduling – program flow mechanisms – system interconnect architecture, performance metrics and measures, parallel processing applications – speed up performance law – Scalability analysis and approaches.

UNIT V – SOFTWARE AND PARALLEL PROCESSING

Parallel programming models – parallel languages and compilers – parallel programming environments – mapping programs onto multicomputers – multiprocessor UNIX design goals – MACH/OS kernel architecture – OSF/I architecture and applications.

REFERENCES

1. Kai Hwang, "Advanced Computer Architecture", TMH 2001.
2. Kai Hwang, Faye.A. Briggs, "Computer Architecture and Parallel processing", McGraw Hill International 1985.
3. William Stallings, Computer Organization and Architecture, McMillan Publishing Company, 1990.
4. M.J. Quinn, "Designing efficient Algorithms for parallel computer", McGraw Hill International, 1994.
5. Richard Y.Kain, "Advanced Computer architecture" – A system design approach", PHI 2003.

112AEPT03 – ADVANCED DIGITAL SIGNAL PROCESSING

AIM

To introduce the students to advanced digital signal processing techniques.

OBJECTIVES

- To introduce the student to basics of signals & systems.
- To study the parametric methods for power spectrum estimation.
- To study adaptive filtering techniques using LMS algorithm and to study the applications of adaptive filtering.
- To study multirate signal processing fundamentals.
- To study the analysis of speech signals.

UNIT I – BASICS OF SIGNALS & SYSTEMS

Sampling Theorem – Quantisation of signalos – Classification of DT systems & Signals – Convoution – correlation – Z-transform – Inverse Z-transform – Properties of DFT Fourier Transform Z-transform.

UNIT II – PARAMETRIC METHODS FOR POWER SPECTRUM ESTIMATION

Relationship between the auto correlation and the model parameters – The Yule – Walker method for the AR Model Parameters – The Burg Method for the AR Model parameters – unconstrained least – squares method for the AR Model parameters – sequential estimation methods for the AR Model parameters – selection of AR Model order.

UNIT III – ADAPTIVE SIGNAL PROCESSING

FIR adaptive filters – steepest descent adaptive filter – LMS algorithm – convergence of LMS algorithms – Application: noise cancellation – channel equalization – adaptive recursive filters – recursive least squares.

UNIT VI – MULTIRATE SIGNAL PROCESSING

Decimation by a factor D – Interpolation by a factor I – Filter Design and implementation for sampling rate conversion: Direct form FIR filter structures – Polyphase filter structure.

UNIT V – SPEECH SIGNAL PROCESSING

Digital models for speech signal: Mechanism of speech production – model for vocal tract, radiation and excitation – complete model – time domain processing of speech signal: - Pitch period estimation – using autocorrelation function – Linear predictive Coding: Basic Principles – autocorrelation method – Durbin recursive solution.

TEXT BOOKS

1. John G.Proakis, Dimitris G. Manobakis, Digital Signal Processing, Principles, Algorithms and Applications, Third edition, (2000) PHI.

2. Monson H.Hayes – Statistical Digital Signal Processing and Modeling, Wiley, 2002.

REFERENCES

1. L.R.Rabiner and R.W.Schaber, Digital Processing of Speech Signals, Pearson Education (1979).

2. Roberto Crist, Modern Digital Signal Processing, Thomson Brooks/Cole (2004).

3. Raghuveer, M. Rao, Ajit S. Bopardikar, Wavelet Transforms, Introduction to Theory and applications, Pearson Education, Asia, 2000.

112AEPT04 – VLSI DESIGN

UNIT I – MANUFACTURING PROCESS

Fabrication steps, Design rules, packaging Integrated circuits, Stick diagram, N well, P well, Twin tub and SOI Process. Interconnects, circuit elements: Resistors, capacitors, Design Hierarchies.

UNIT II – MOS TRANSISTOR THEORY

NMOS, PMOS Enhancement transistor, Threshold voltage, Body effect, MOS DC equations, channel length modulation, Mobility variation, MOS models, small signal AC characteristics, complementary CMOS inverter DC characteristics, Noise Margin, Rise time, fall time, power dissipation, transmission gate, tristate inverter.

UNIT III – CMOS INVERTER

CMOS inverter, static behavior, Performance of CMOS inverter, Power, Energy and Energy delay.

UNIT IV – CMOS COMBINATIONAL AND SEQUENTIAL DESIGN

Static and Dynamic CMOS combinational design, Static Latches and Registers, Dynamic latches and Registers, Non bistable sequential circuits.

UNIT V - DESIGN ISSUES AND TESTING

Parasitics, Timing issues, Need for testing, manufacturing test principles, Design strategies for test, Chip level and system level test techniques.

TEXT BOOKS

1. Jan Rabey, Digital Integrated circuits, Pearson Education 2004.

REFERENCES

1. M.J.S.Smith, Application Specific integrated circuits, Pearson Education, 1997.
2. Wayne Wolf, Modern VLSI Design, Pearson Education 2003.
3. E. Fabricious, Introduction to VLSI design, McGraw-Hill 1990.

112AEPT05 - COMPUTER COMMUNICATIONS AND NETWORKING

BUILDING A NETWORK: Requirements: Connectivity, Cost effective resource sharing, support for common services – Network Architecture: Layering and protocols, OSI architecture, Internet architecture – Implementing network software: Application Programming Interface, Protocol Implementation issues – Performance: Bandwidth and Latency, Product of Delay and Bandwidth, High Speed Networks.

SWITCHING AND ROUTING IN NETWORKS: Framing – Error Detection – IEEE Standards: Ethernet, Rings, Wireless – Telephone switching systems: Electro Mechanical Systems, Stored program control systems – Message switching – Packet switching – Packet switching support to Circuit switching networks – Cell switching: Cells, segmentation and reassembly, virtual paths, physical layers for ATM.

INTERNET WORKING: Simple Internetworking (IP): Service Model, Global addresses, Data forwarding in IP, Address Translation (ARP), Host Configuration (DHCP), Error Reporting (ICMP), Virtual Networks and Tunnels – Routing: Network as a graph, Distance Vector, Metrics.

END – TO – END PROTOCOLS: Simple Demultiplexer (UDP) – Reliable Byte stream (TCP): End to End issues, Segment Format, Connection Establishment and Termination, sliding window, triggering transmission, adaptive retransmission, record boundaries, TCP extension, Alternative design choices – Remote Procedure Call: Fundamentals, Implementation – Transport for Real Time Applications: Requirements, RTP details, control protocols.

NETWORK SECURITY & APPLICATIONS: NETWORK SECURITY – Threats, Introduction to cryptography, Firewalls – Applications – Electronic Mail (SMTP, MINE, IMAP), World Wide Web (HTTP), Name services, Network Management – Web services: Custom Application Protocols (WSDL, SOAP) – Multimedia Applications: Session Control and Call Control, Resource allocation for multimedia applications.

TEXT BOOKS:

1. "Computer Networks: A Systems Approach", Larry L. Peterson and Bruce S. Davie, 4th Edition, Morgan Kaufmann Publishers, 2007.
2. "Computer Networks Protocols, Standards and Interfaces", Uyless Black, Second Edition, Prentice Hall of India.

REFERENCES:

1. "Computer Nerworks", Andrew S. Tanenbaum, Prentice Hall India Private Limited, 4th Edition, 2005.
2. "Data Comunications and Networking", Behrouz A. Forouzan, Tata Mc Graw Hill publications, 4th Edition.

112AEPT06 - ADVANCED MICRO PROCESSORS AND MICROCONTROLLERS

1. THE INTEL X86 FAMILY

The Intel X86 family architecture, 32 bit processor evolutions Systems connections and timing, Instruction and data formals, Instruction set of X86 processors, Addressing modes.

2. INTEL X86 ASSEMBLY LANGUAGE PROGRAM

Implementation of strings, Procedures, Macros, BIOS using X86 assembly language programming, Memory and I/O interfacing, Anolog interfacing and industrial control.

3. SYSTEM DEVELOPMENT

Microprocessors based system design, Microcontroller 8051, 8051 based system design.

4. RENESAS R8C 16 BIT MICROCONTROLLER

The R8C Architecture, CPU registers, Instruction Set, On Chip Peripherals, R8C Tiny Development tools, ADC, PWM, UART, Timer interrupts. System design using R8C Microcontroller.

5. RISC PROCESSORS

RISC vs CISC, RISC properties and evolution, Advanced RISC microprocessors, The power PC family, The SUN SPARC family, The MIPS RX 100 family.

REFERENCES

1. B.B Bery, "The INTEL Microprocessors 80186/80188, 80286, 80386, 80486, PENTIUM, and PENTIUM pro processor, Pentium II, III, 4, 7/E", Prentice Hall, 2006.
2. K. Udayakumar, B.S. Uma Shankar, "Advanced Microprocessors and IBM PC assembly language programming", Tata McGraw-Hill, 1996.
3. "R8C Tiny Group Manual", Published by Renesas System solutions Asia Pvt. Ltd., Singapore, 2005.
4. "Embedded system design using R8C Tiny microcontroller", Published by Renesas System solutions Asia Pvt. Ltd., Singapore, 2005.
5. Daniel Tabak, "Advanced Microprocessors – Theory and Application: Intel and Motorola", Prentice Hall, 1992.
6. Rafiquzzaman.M, "Microprocessors – Theory and Application: Intel and Motorola", Prentice Hall, 1992.
7. Kenneth J. Ayala, "The 8051 Microcontroller, Architecture, Programming and Applications", Penram International Publishing (India), 1996.

II SEMESTER
212AEPT01 - ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

UNIT I MODELS FOR INTERGRATED CIRCUIT ACTIVE DEVICES

Depletion region of a PN junction – large signal behavior of bipolar transistors – small signal model of bipolar transistor – large signal behavior of MOSFET – small signal model of the MOS transistors – short channel effects in MOS transistors – weak inversion in MOS transistors – substrate current flow in MOS transistor.

UNIT II CIRUIT CONFIGURATION FOR LINEAR IC

Current sources, Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages.

UNIT III OPERATIONAL AMPLIFIERS

Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise.

UNIT IV ANALOG MULTIPLIER AND PLL

Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise – Noise models of Integrated – circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

UNIT V ANALOG DESIGN WITH MOS TECHNOLOGY

MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source – CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic – Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

REFERENCES:

1. Gray, Meyer, Lewis, Hurst, "Analysis and design of Analog IC's", Fourth Edition, Willey International, 2002.
2. Behzad Razavi, "Principles of data conversion system design", S. Chand and company ltd, 2000.
3. Nandita Dasgupta, Amitava Dasgupta, "Semiconductor Devices, Modelling and Technology", Prentice Hall of India Pvt. Ltd, 2004.
4. Gerebene, Bipolar and MOS Analog Integrated circuit design", John Wiley & sons, Inc., 2003.
5. Phillip E. Allen Douglas R. Holberg, "CMOS Analog Circuit Design", Second Edition – Oxford University Press-2003.

212AEPT02 - ADVANCED DIGITAL SYSTEM DESIGN

UNIT I SEQUENTIAL CIRCUIT DESIGN

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart – ASM Realization.

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built – in Self Test.

UNIT IV SYNCHRONOUS DESIGN USING PROGRAMMABLE DEVICES

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD – FPGA – Xilinx FPGA – Xilinx 2000 – Xilinx 3000.

UNIT V SYSTEM DESIGN USING VHDL

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers – Counters – Sequential Machine – Combinational Logic Circuits – VHDL Code for – Serial Adder, Binary Multiplier – Binary Divider – complete Sequential Systems – Design of a Simple Microprocessor.

REFERENCES:

1. Donald G. Givone "Digital principles and Design" Tata McGraw Hill 2002.
2. John M Yarbrough "Digital Logic applications and Design" Thomson Learning, 2001.
3. Nripendra N Biswas "Logic Design Theory" Prentice Hall of India, 2001.
4. Charles H. Roth Jr. "Digital System Design using VHDL" Thomson Learning, 1998.
5. Charles H. Roth Jr. "Fundamentals of Logic design" Thomson Learning, 2004.
6. Stephen Brown and Zvonk Vranesic "Fundamentals of Digital Logic with VHDL Design" Tata McGraw Hill, 2002.
7. Navabi.Z. "VHDL Analysis and Modeling of Digital Systems McGraw International, 1998.
8. Parag K Lala, "Digital System design using PLD" BS Publications, 2003.
9. Peter J Ashendem, "The Designers Guide to VHDL" Harcourt India Pvt Ltd, 2002.
10. Mark Zwolinski, "Digital System Design with VHDL" Pearson Education, 2004.
11. Skahill. K, "VHDL for Programmable Logic" Pearson education, 1996.

212AEPT03 - DIGITAL CONTROL ENGINEERING

UNIT I

Review of frequency and time response analysis and specifications of control systems, need for controllers, continues time compensations, continues time PI, PD, PID controllers, digital PID controllers.

UNIT II SIGNAL PROCESSING IN DIGITAL CONTROL

Sampling, time and frequency domain description, aliasing, hold operation, mathematical model of sample and hold, zero and first order hold, factors limiting the choice of sampling rate, reconstruction.

UNIT III MODELING AND ANALYSIS OF SAMPLED DATA CONTROL SYSTEM

Difference equation description, Z-transform method of description, pulse transfer function, time and frequency response of discrete time control systems, stability of digital control systems, Jury's stability test, state variable concepts, first companion, second companion, Jordan canonical models, discrete state variable models, elementary principles.

UNIT IV DESIGN OF DIGITAL CONTROL ALGORITHMS

Review of principle of compensator design, Z-plane specifications, digital compensator design using frequency response plots, discrete integrator, discrete differentiator, development of digital PID controller, transfer function, design in the Z-plane.

UNIT V PRACTICAL ASPECTS OF DIGITAL CONTROL ALGORITHMS

Algorithm development of PID control algorithms, software implementation, implementation using microprocessors and microcontrollers, finite word length effects, choice of data acquisition systems, microcontroller based temperature control systems, microcontroller based motor speed control systems.

REFERENCES

1. M.Gopal, "Digital Control and Static Variable Methods", Tata McGraw Hill, New Delhi, 1997.
2. John J. D'Azzo, "Constantive Houpios, Linear Control System Analysis and Design", McGraw Hill, 1995.
3. Kenneth J. Ayala, "The 8051 Microcontroller – Architecture, Programming and Applications", Penram International, 2nd Edition, 1996.

212AEPT04 - EMBEDDED SYSTEMS

UNIT I EMBEDDED ARCHITECTURE

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design. Embedded system design process – Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design – Structural Description, Behavioral Description, Design Example: Model Train Controller.

UNIT II EMBEDDED PROCESSOR AND COMPUTING PLATFORM

ARM processor – processor and memory organization, Data operations, Flow of Control, SHARC processor – Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example: Alarm Clock.

UNIT III NETWORKS

Distributed Embedded Architecture – Hardware and Software Architectures, Networks for embedded systems – 12C, CAN Bus, SHARC link pports, Ethernet, Myrinet, Internet, Network – Based design – Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS

Clock driven Approach, weighted round robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off-line Versus On-line scheduling.

UNIT V SYSTEM DESIGN TECHNIQUES

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX – System Architecture, Ink jet printer – Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

REFERENCES

1. Wayne Wolf, Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufman Publishers, 2001.
2. Jane. W.S. Liu Real-Time systems, Pearson Education Asia, 2000.
3. C.M. Krishna and K.G. Shin, Real-Time Systems, McGraw-Hill, 1997.
4. Frank Vahid and Tony Givargi Embedded System Design: A Unified Hardware/Software Introduction, S, John Wiley & Sons, 2000.

212AEPT05 - HIGH PERFORMANCE COMMUNICATION NETWORKS

UNIT I PACKET SWITCHED NETWORKS

OSI and IP models, Ethernet (IEEE 802.3), Token ring (IEEE 802.5), Wireless LAN (IEEE 802.11) FDDI, DQDB, SMDS: Internetworking with SMDS

UNIT II ISDN AND BROADBAND ISDN

ISDN – overview, interfaces and functions, Layers and services – Signaling System 7 – Broadband ISDN architecture and Protocols.

UNIT III ATM AND FRAME RELAY

ATM: Main features – addressing, signaling and routing, ATM header structure – adaptation layer, management and control, ATM switching and transmission.
Frame Relay: Protocols and services, Congestion control, Internetworking with ATM, Internet and ATM, Frame relay via ATM.

UNIT IV ADVANCED NETWORK ARCHITECTURE

IP forwarding architectures overlay model, Multi Protocol Label Switching (MPLS), integrated services in the Internet, Resource Reservation Protocol (RSVP), Differentiated services.

UNIT V BLUE TOOTH TECHNOLOGY

The Blue tooth module – Protocol stack Part I: Antennas, Radio interface, Base band, The Link controller, Audio, The Link Manager, The Host controller interface; The Blue tooth module – Protocol stack Part I: Logical link control and adaptation protocol, RFCOMM, Service discovery protocol, Wireless access protocol, Telephony control protocol.

REFERENCES

1. William Stallings, "ISDN and Broadband ISDN with Frame Relay and ATM", 4th Edition, Pearson education Asia, 2002.
2. Leon Gracia, Widjaja, "Communication networks", Tata McGraw-Hill, New Delhi, 2000.
3. Jennifer Kasera, Pankaj Sethi, "ATM Networks", Tata McGraw-Hill, New Delhi, 2000.
4. Ranier Handel, Manfred N.Huber, Stefan Schroder, "ATM Networks", 3rd edition, Pearson education asia, 2002.
5. Jean Walrand and Pravin varaiya, "High Performance Communication Networks", 2nd edition, Harcourt and Morgan Kauffman, London 2000.
6. William Stallings, "High-speed Networks and Internets", 2nd edition, Pearson education Asia, 2003.

212AEPT06 - DIGITAL IMAGE PROCESSING

UNIT I - DIGITAL IMAGE FUNDAMENTALS

Elements of digital image processing systems, Elements of visual perception, psycho visual model, brightness, contrast, hue, saturation, mach band effect, Color image fundamentals – RGB, HSI models, Image sampling, Quantization, dither, Two-dimensional mathematical preliminaries.

UNIT II - IMAGE TRANSFORMS

ID DFT, 2D transforms – DFT, DCT, Discrete Sine, Watch, Hadamard, Slant, Hear, KLT, SVD, Wavelet Transform.

UNIT III - IMAGE ENHANCEMENT AND RESTORATION

Histogram modification and specification techniques, Noise distributions, Spatial averaging, Directional Smoothing, Median, Geometric mean, Harmonic mean, Contraharmonic and Yp mean filters, Homomorphic filtering. Color image enhancement. Image Restoration – degradation model, Unconstrained and Constrained restoration, Inverse filtering – removal of blur caused by uniform linear motion, Wiener filtering, Geometric transformations – Spatial transformations , Gray – Level interpolation.

UNIT IV - IMAGE SEGMENTATION AND RECOGNITION

Edge detection. Image segmentation by region growing, region splitting and merging, edge linking. Image Recognition – Patterns and pattern classes, Matching by minimum distance classifier, Matching by correlation, Back Propagation Neural Network, Neural Network applications in Image Processing.

UNIT V - IMAGE COMPRESSION

Need for data compression, Huffman, Run Length Encoding, Shift codes, Arithmetic coding, Vector Quantization, Block Truncation Coding. Transform Coding – DCT and Wavelet. JPEG, MPEG, Standards, Concepts of Context based Compression.

REFERENCES:

1. Rafael C. Gonzalez., Richard E.Woods, 'Digital Image Processing', Pearson Education, Inc., Second Edition, 2004.
2. Anil K. Jain, 'Fundamentals of Digital Image Processing', Prentice Hall of India, 2002.
3. David Salomon: Data Compression – The Complete Reference, Springer Verlag New York Inc., 2nd Edition, 2001.
4. Rafael C. Gonazalez, Richard E. Woods, Steven Eddins, 'Digital Image Processing using MATLAB', Pearson Education, Inc., 2004.
5. William K.Pratt, 'Digital Image Processing', John Wiley, New York, 2002.
6. Milman Sonka, Vaclav Hlavac, Roger Boyle, 'Image Processing, Analysis, and Machine Vision', Brooks/Cole, Vikas Publishing House, II ed., 1999.
7. Sid Ahmed, M.A., 'Image Processing Theory, Algorithms and Architectures', McGraw-Hill, 1995.

ELECTRONIC DESIGN LAB II

1. System design using PLL.
2. System design using CPLD.
3. Alarm clock using embedded micro controller.
4. Model train controller using embedded micro controller.
5. Elevator controller using embedded micro controller.
6. Simulation of Non adaptive Digital Control System using MAT LAB control system toolbox.
7. Simulation of Adaptive Digital Control System using MAT LAB control system toolbox.

III SEMESTER

312AEPT01 -ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN

EMI/EMC CONCEPTS
EMI-EMC definitions and Units of parameters; Sources and victim of EMI: Conducted and Radiated EMI Emission and Susceptibility; Transient EMI, ESD; Radiation Hazards.

EMI COUPLING PRINCIPLES
Conducted, radiated and transient coupling; Common ground impedance coupling; Common mode and ground loop coupling; Differencial mode coupling; Near field cable to cable coupling, cross talk; Field to cable coupling; Power mains and Power supply coupling.

EMI CONTROL TECHNIQUES
Shielding, Filtering, Grounding, Bonding, Isolation transformer, Transient suppressors, Cable routing, Signal control.

EME DESIGN OF PCBS
Component selection and mounting; PCB trace impedance; Routing; Cross talk control; Power distribution decoupling; Zoning; Grounding; Vias connection; Terminations.

EMI MEASUREMENTS AND STANDARDS
Open area test site; TEM cell; EMI test shielded chamber and shielded ferrite lined anechoic chamber; Tx /Rx Antennas, Sensors, Injectors / Couplers, and coupling factors; EMI Rx and spectrum analyzer, Civilian standards-CISPR, FCC, IEC, EN; Military standards-MIL461E/462.

REFERENCE

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312AEPT02 – WIRELESS NETWORKS

1. WIRELESS ACCESS

Medium Access Alternatives: Fixed – Assignment for Voice Oriented Nertworks Random Access for Data Oriented Networks – Integration of voice and data traffic.

2. WIRELESS NETWORK FUNDAMENTALS

Principles of Wireless Network Operation: Wireless Network Topologies – Cellular Topology – Cell fundamentals – Signal to interference ratio calculation – Capacity expansion techniques – Network planning for CDMA systems – Mobility management – Radio resources and power management – Security in Wireless networks.

3. WIRELESS WANS

Communication in the infrastructures – Reference architecture for North American Systems – GSM, CDMA – IMT 2000 – The Data Oriented CDPD Network – GPRS and High Data rates – Short Messaging Service in GSM – Mobile Application Protocols.

4. WLANS AND HIPERLANS

Introduction to wireless LANs – IEEE 802.11 WLANs – Physical Layer – MAC sublayer– MAC Management Sublayer– Wireless ATM – HIPERLAN– HIPERLAN-2.

5. ADHOC NETWORKING

IEEE 802.15.WP AN – Home RF Bluetooth – Wireless Geolocation System – Architecture – Technologies for Wireless Geolocation Standards – Performance Measures for Geolocation Systems.

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1. Kaveth Pahlavan, K. Prashanth Krishnamuorthy, "Principles of Wireless Networks", Pearson Education Asia, 2002.
2. Leon Garcia, Widjaja, "Communication Networks", Tata McGraw Hill, New Delhi 2000.
3. William Stallings, "Wireless Communications and networks" Prentice Hall, 2002.

312AEPT03 – NEUTRAL NETWORKS AND ITS APPLICATIONS

1. INTRODUCTION TO ARTIFICIAL NEURAL NETWORKS

Neuro-physiology – General Processing Elemen – ADALINE – LMS learning rule – MADALINE – MR2 training algorithm.

2. BPN AND BAM

Back Propagation Network – updating of output and hidden layer weights – application of BPN – associative memory – Bi-directional Associative Memory – Hopfield memory – travelling sales man problem.

3. SIMULATED ANNEALING AND CPN

Annealing, Boltzmann machine – learning – application – Counter Propagation network – architecture – training – Applications.

4. SOM AND ART

Self organizing map – learning algorithm – feature map classifier – applications – architecture of Adaptive Resonance Theory – pattern matching in ART network.

5. NEOCOGNITRON

Architecture of Neocognitron – Data processing and performance of architecture of spacio – temporal networks for speech recognition.

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2. Laurene Fauselt, "Fundamentals of Neural Networks: Architecture, Algorithms and Applications", Prentice Hall, 1994.

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